

WHAT IS CLAIMED IS

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1. A substrate to be mounted with a semiconductor chip, comprising:

10 a plurality of insulation layers forming a laminated structure, said laminated structure having a chip-mounting surface on which a semiconductor chip is mounted; and

a built-in capacitor formed in said laminated structure, said built-in capacitor being integrated with said laminated structure,

15 said built-in capacitor comprising a dielectric film and a pair of electrode layers sandwiching said dielectric film.

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2. The substrate as claimed in claim 1, wherein said insulation layer forming said chip-mounting surface is formed of a baked organic
25 polysilane layer.

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3. The substrate as claimed in claim 2, wherein said baked organic polysilane layer comprises a baked polymethylphenyl silane layer.

4. The substrate as claimed in claim 2,
5 wherein said baked organic polysilane layer has a
silicon skeleton and an organic substituent at a side
chain of said skeleton.

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5. The substrate as claimed in claim 2,
wherein said baked organic polysilane layer has a
thermal expansion coefficient of about 2.6ppm/K at
15 said mounting surface.

20 6. The substrate as claimed in claim 2,
wherein said baked organic polysilane layer has a
Young modulus of about 1.2GPa.

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7. The substrate as claimed in claim 2,
wherein said baked organic polysilane layer has a
dielectric loss tangent of about 0.005.

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8. The substrate as claimed in claim 2, wherein said baked organic polysilane is baked at a temperature of 230°C or higher.

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9. The substrate as claimed in claim 1, wherein said substrate includes power feeding
10 conductor and a ground conductor, and wherein said built-in capacitor is provided in electrical connection between said ground conductor and said power feeding conductor.

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10. The substrate as claimed in claim 9, wherein each of said power feeding conductor and said
20 ground conductor extends continuously from a bottom surface of said substrate to a top surface of said substrate along a via-hole.

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11. The substrate as claimed in claim 10, wherein each of said power feeding conductor and said ground conductor has a projecting part projecting from
30 said chip-mounting surface.

12. The substrate as claimed in claim 11,
wherein said projecting part extends laterally beyond
a diameter of said via-hole along said chip-mounting
5 substrate.

10 13. The substrate as claimed in claim 11,
wherein said projecting part has a rounded shape and
extends laterally beyond a diameter of said via-hole
in intimate contact with said chip-mounting surface.

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14. The substrate as claimed in claim 1,
wherein said capacitor is formed between a first
20 insulation layer and a second insulation layer formed
on said first insulation layer in intimate contact
with both of said first and second insulation layers,
said first and second insulation layers being included
in said plural insulation layers, one of said first
25 and second insulation layers providing said chip-
mounting surface and being formed of a baked organic
polysilane layer.

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15. A substrate to be mounted with a
semiconductor chip, comprising:

a plurality of insulation layers forming a laminated structure, said laminated structure having a chip-mounting surface on which a semiconductor chip is mounted; and

5 first and second built-in capacitors each formed in said laminated structure at a first side and a second side of an insulation layer formed of a baked organic polysilane layer, each of said first and second built-in capacitors being integrated with said
10 laminated structure,

each of said first and second built-in capacitors comprising a dielectric film and a pair of electrode layers sandwiching said dielectric film,

said first and second built-in capacitors
15 being connected parallel with each other between a power feed path and a ground path extending continuously through said substrate from a bottom surface thereof to a top surface thereof.

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16. A method of manufacturing a substrate to be mounted with a semiconductor chip, said substrate
25 comprising plurality of insulation layers forming a laminated structure and a capacitor provided in said laminated structure,

said method comprising the steps of:

forming said laminated structure by
30 laminating said insulation films consecutively, said insulation films including a first insulation film and a second insulation film formed on said first insulation film,

wherein there are provided the steps, after forming said first insulation layer but before forming said second insulation layer, of: forming a first electrode film; forming a dielectric film on said first electrode film; and forming a second electrode film on said dielectric film.

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17. The method as claimed in claim 16, wherein said step of forming said laminated structure comprises the steps of:

forming a layer of organic polysilane;
pre-baking said layer of organic polysilane;
forming a via-hole in said organic polysilane; and

post-baking said layer of organic polysilane such that said layer of organic polysilane is converted to a baked organic polysilane layer, said step of post-baking being conducted at a temperature of 230°C or higher.

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18. The method as claimed in claim 17, wherein said step of post-baking is conducted at a temperature of 500°C or higher.

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19. The method as claimed in claim 17,
wherein said step of pre-baking is conducted at a
temperature of about 120°C.

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20. The method as claimed in claim 16,
wherein said step of forming said dielectric film
10 comprises an anodization process of said first
electrode film.